Claims

What is claimed is:

1. A method for implementing enhanced performance with reduced quiescent power dissipation using mixed threshold CMOS devices in latch circuit designs comprising the steps of:

identifying logic blocks in critical data and clock paths of a latch circuit;

substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor for use in said identified logic blocks in the critical data and clock paths; and

selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors.

2. A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 includes the steps of providing RVT transistors to implement output buffer transistors.

3. A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein the step of identifying logic blocks in critical data and clock paths of the latch circuit includes the steps of identifying logic blocks used in loading data into the latch circuit.

4. A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 3 includes the steps of identifying logic blocks used in each data clock stage.

5. A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein the step of selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying logic blocks used only during testing in the latch circuit; and selectively implementing the identified logic blocks used only during testing with RVT transistors, or low leakage (LLD) transistors.

6. A method for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 1 wherein the step of selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying logic blocks used to maintain the contents of latches in the latch circuit; and selectively implementing the identified logic blocks used to maintain the contents of latches with RVT transistors, or low leakage (LLD) transistors.

7. A latch circuit for implementing enhanced performance with reduced quiescent power dissipation comprising:

critical data and clock paths;

non-critical sections;

a low voltage threshold (LVT) transistor being used only in said critical data and clock paths; and

said non-critical sections being implemented with regular voltage threshold (RVT) transistors, or low leakage (LLD) transistors.

8. A latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 includes said RVT transistors used for output buffer transistors.

9. A latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 wherein said critical data and clock paths include multiple critical path logic blocks, each critical path logic block implemented with said LVT transistors.

10. A latch circuit for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 7 wherein said non-critical sections include logic blocks used for testing and to maintain the contents of latches in the latch circuit.

11. A computer program product for implementing enhanced performance with reduced quiescent power dissipation using mixed threshold CMOS devices in latch circuit designs in a computer system, said computer program product including instructions executed by the computer system to cause the computer system to perform the steps of:

identifying logic blocks in critical data and clock paths of a latch circuit;

substituting a low voltage threshold (LVT) transistor to replace each regular voltage threshold (RVT) transistor for use in said identified logic blocks in the critical data and clock paths; and

selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors.

12. A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11 includes the steps of providing RVT transistors to implement output buffer transistors.

13. A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11 wherein the step of identifying logic blocks in critical data and clock paths of the latch circuit includes the steps of identifying logic blocks used in loading data into the latch circuit.

14. A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 13 includes the steps of identifying logic blocks used in a data clock stage.

15. A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11 wherein the step of selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying logic blocks used only during testing in the latch circuit; and selectively implementing the identified logic blocks used only during testing with RVT transistors, or low leakage (LLD) transistors.

16. A computer program product for implementing enhanced performance with reduced quiescent power dissipation as recited in claim 11 wherein the step of selectively implementing non-critical sections of the latch circuit with RVT transistors, or low leakage (LLD) transistors includes the steps of identifying logic blocks used to maintain the contents of latches in the latch circuit; and selectively implementing the identified logic blocks used to maintain the contents of latches with RVT transistors, or low leakage (LLD) transistors.